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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
YEUNG LOPEZ, FEIFEI	
ART UNIT	PAPER NUMBER
2826	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/582,833	PEKKARINEN ET AL.	
	Examiner	Art Unit	
	FEI FEI YEUNG LOPEZ	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 April 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on April 23, 2009 has been entered.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 4, 5, 8, 11, 12,15, 16,19, 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Hong et al (US Patent 5,889,308).

4. Regarding claim 1, Hong teaches a semiconductor component, comprising a semiconductor element (layer 102 in fig. 4) encased by a cover element (element a) having an integrated electroconductive metal element (layer 105) comprising at least one outlet, wherein the at least one outlet is configured to connect the electroconductive metal element to ground in order to shield the semiconductor element against electrostatic pulses (column 4, lines 43-57).

5. Regarding claim 4, Hong teaches a semiconductor component according to claim 1, wherein the electroconductive metal element forms a permanent, integrated part of the semiconductor component (see fig. 4).

6. Regarding claim 5, Hong teaches a semiconductor component according to claim 4 claim 1, wherein the electroconductive metal element (layer 105) is placed underneath the cover element of the semiconductor component, inside said cover element (element a in fig. 4).

7. Regarding claim 8, Hong teaches a method for shielding a semiconductor element against electrostatic pulses, comprising: integrating the semiconductor element in a semiconductor component (layer 102 in fig. 4), covering the semiconductor element with a cover element (element a), integrating an electroconductive metal element (layer 105) within the cover element of the semiconductor component and providing at least one outlet for the integrated electroconductive metal element, so that the at least one outlet is configured to connect the electroconductive metal element to ground (column 4, lines 43-57).

8. Regarding claim 11, Hong teaches a method according to claim 8, wherein the electroconductive metal element is integrated as a permanent part of the semiconductor component (see fig. 4).

9. Regarding claim 12, Hong teaches a method according to claim 11, wherein the electroconductive metal element is integrated underneath the cover element of the semiconductor component, inside said cover element (see fig. 4).

10. Regarding claim 15, Hong teaches an arrangement including a mounting tray and at least one semiconductor component, wherein said at least one semiconductor component comprises a semiconductor element (layer 102 in fig. 4) encased by a cover element (layer a) having an integrated electroconductive metal element (layer 105), where the electroconductive metal element is provided with at least one outlet that is grounded to a ground plane of the mounting tray (column 4, lines 43-57).

11. Regarding claim 16, Hong teaches apparatus for shielding a semiconductor element against electrostatic pulses, comprising: means for covering (layer a in fig. 4) the semiconductor element in a semiconductor component (layer 102) having an integrated electroconductive metal element (layer 105); and means for providing at least one outlet for the integrated electroconductive metal element, so that the at least one outlet is configured to connect the electroconductive metal element to ground (column 4, lines 43-57).

12. Regarding claim 19, Hong teaches the apparatus of claim 16, wherein the electroconductive metal element is integrated as a permanent part of the semiconductor component (see fig. 4).

13. Regarding claim 20, Hong teaches the apparatus of claim 16, wherein the electroconductive metal element is integrated underneath the cover element of means for covering the semiconductor component, inside said cover element (see fig. 4).

14. Claims 1, 2, 4-9,11-14,16, 17,19, 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Sherwood et al (US Patent 4,303,960).

15. Regarding claim 1, Sherwood teaches a semiconductor component, comprising a semiconductor element (MOS in layer 103 in fig. 3) encased by a cover element (encased by layer 22 in fig. 1 and the substrate the MOS is formed) having an integrated electroconductive metal element (layer 75) comprising at least one outlet, wherein the at least one outlet is configured to connect the electroconductive metal element to ground in order to shield the semiconductor element against electrostatic pulses (column 4, lines 59-65).

16. Regarding claim 2, Sherwood teaches a semiconductor component according to claim 1, wherein in structure, the electroconductive metal element is a planar sheet (column 3, lines 43-46).

17. Regarding claim 4, Sherwood teaches a semiconductor component according to claim 1, wherein the electroconductive metal element forms a permanent, integrated part of the semiconductor component (see fig. 1).

18. Regarding claim 5, Sherwood teaches a semiconductor component according to claim 4 claim 1, wherein the electroconductive metal element (layer 75 in figs 1 and 3) is placed underneath the cover element (when "the cover element" in claim 1 is interpreted as to be formed by layers 21 and 22) of the semiconductor component, inside said cover element.

19. Regarding claim 6, Sherwood teaches a semiconductor component according to claim 1, wherein the electroconductive metal element (layer 75 in fig. 3) is placed on top of attached to the cover element of the semiconductor component, outside said cover

element (layer 75 is outside of "the cover element" formed by layer 22 and the substrate the MOS is formed (layer 103)).

20. Regarding claim 7, Sherwood teaches a semiconductor component according to claim 1, wherein the electroconductive metal element is induced in the cover element of the semiconductor component either chemically or electrochemically (column 3, lines 43-52, where Sherwood teaches using glue to bond layer 75 to the device. The bonding force of the glue is generated by molecular force of the glue—thus, induced chemically). Also, how the electroconductive metal element is formed, whether chemically, electrochemically, or other process, does not carry patentable weight in a device claim. "[E]ven though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process." In re Thorpe, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985). See MPEP 2113.

21. Regarding claim 8, Sherwood teaches a method for shielding a semiconductor element against electrostatic pulses, comprising: integrating the semiconductor element in a semiconductor component (MOS in layer 103, see fig. 3), covering the semiconductor element with a cover element (cover element formed by layers 22 and layer 103), integrating an electroconductive metal element (layer 75 in figs. 1 and 3) within the cover element of the semiconductor component and providing at least one

outlet for the integrated electroconductive metal element, so that the at least one outlet is configured to connect the electroconductive metal element to ground (column 4, lines 59-65).

22. Regarding claim 9, Sherwood teaches a method according to claim 8, wherein in the semiconductor component, there is integrated an electroconductive, planar metal element (layer 75 in fig. 3).

23. Regarding claim 11, Sherwood teaches a method according to claim 8, wherein the electroconductive metal element (layer 75 see figs. 1 and 3) is integrated as a permanent part of the semiconductor component.

24. Regarding claim 12, Sherwood teaches a method according to claim 11, wherein the electroconductive metal element (layer 75 in figs. 1 and 3) is integrated underneath the cover element (when the cover element is formed by layers 21 and 22 in fig. 1) of the semiconductor component, inside said cover element.

25. Regarding claim 13, Sherwood teaches a method according to claim 11, wherein the electroconductive metal element (layer 75 in fig. 3) is integrated on top of by attachment to the cover element of the semiconductor component, outside said cover element (layer 75 is outside of the cover element formed by layer 22 and layer 103 in fig. 3).

26. Regarding claim 14, Sherwood teaches a method according to claim 8, wherein the electroconductive element is induced in the cover element of the semiconductor component either chemically or electrochemically (column 3, lines 43-52, where

Sherwood teaches using glue to bond layer 75 to the device. The bonding force of the glue is generated by molecular force of the glue—thus, induced chemically).

27. Regarding claim 16, Sherwood teaches apparatus for shielding a semiconductor element against electrostatic pulses, comprising: means for covering (layers 21 and 22) the semiconductor element in a semiconductor component (MOS on layer 103) having an integrated electroconductive metal element (layer 75 in fig. 3); and for providing at least one outlet for the integrated electroconductive metal element, so that the at least one outlet is configured to connect the electroconductive metal element to ground (column 4, lines 59-65).

28. Regarding claim 17, Sherwood teaches the apparatus of claim 16, wherein in the semiconductor component, there is integrated an electroconductive, planar metal element (layer 75 in fig. 3).

29. Regarding claim 19, Sherwood teaches the apparatus of claim 16, wherein the electroconductive metal element (layer 75 in figs. 1 and 3) is integrated as a permanent part of the semiconductor component.

30. Regarding claim 20, Sherwood teaches the apparatus of claim 16, wherein the electroconductive metal element (layer 75 in figs. 1 and 3) is integrated underneath the cover element of means for covering the semiconductor component, inside said cover element.

31. Claims 1, 3, 8, 10, 16 and 18 are rejected under 35 U.S.C. 102(b) as being anticipated by Wu et al (US Patent 6,175,394 B1).

32. Regarding claim 1, Wu teaches a semiconductor component, comprising a semiconductor element (layer 20 in fig. 1) encased by a cover element (cover of the display panel) having an integrated electroconductive metal element (layer 24, see column 2, lines 28-30) comprising at least one outlet, wherein the at least one outlet is configured to connect the electroconductive metal element to ground (column 7, lines 6-65) in order to shield the semiconductor element against electrostatic pulses.

33. Regarding claim 3, Wu teaches a semiconductor component according to claim 1, wherein the electroconductive metal element is a thin loop structure (see fig. 1).

34. Regarding claim 8, Wu teaches a method for shielding a semiconductor element against electrostatic pulses, comprising: integrating the semiconductor element (layer 20 in fig. 1) in a semiconductor component, covering the semiconductor element with a cover element (cover of the display panel), integrating an electroconductive metal element (layer 24 in fig. 1) within the cover element of the semiconductor component and providing at least one outlet for the integrated electroconductive metal element, so that the at least one outlet is configured to connect the electroconductive metal element to ground (column 7, lines 61-65).

35. Regarding claim 10, Wu teaches a method according to claim 8, wherein in the semiconductor component, there is integrated an electroconductive, loop-shaped metal element (layer 24 in fig. 1).

36. Regarding claim 16, Wu teaches apparatus for shielding a semiconductor element against electrostatic pulses, comprising: means for covering the semiconductor element in a semiconductor component (layer 20 in fig. 1) having an integrated

electroconductive metal element (layer 24); and means for providing at least one outlet for the integrated electroconductive metal element, so that the at least one outlet is configured to connect the electroconductive metal element to ground (column 7, lines 61-65).

37. Regarding claim 18, Wu teaches the apparatus of claim 16, wherein in the semiconductor component, there is integrated an electroconductive, loop-shaped metal element (layer 24 in fig. 1).

Response to Arguments

38. Applicant's arguments filed on April 23, 2009 have been fully considered but they are not persuasive. Hong teaches an "elecrtroconductive metal element" (layer 105 in fig. 4) as claimed in amended claim 1 (see rejection above).

39. Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to FEI FEI YEUNG LOPEZ whose telephone number is (571)270-1882. The examiner can normally be reached on 7:30am-5:00pm Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue Purvis can be reached on 571-272-1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Feifei Yeung-Lopez/
Examiner, Art Unit 2826

/Minh-Loan T. Tran/
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Art Unit 2826